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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/671,984	09/26/2003	Brian Allan Floyd	YOR920030428US1	8861

7590 12/29/2004

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EXAMINER	
CHOE, HENRY	
ART UNIT	PAPER NUMBER
2817	

DATE MAILED: 12/29/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/671,984	FLOYD, BRIAN ALLAN	
	Examiner	Art Unit	
	Henry K Choe	2817	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 September 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7 and 9-15* is/are rejected.

7)☒ Claim(s) *8* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *10/27/2003*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-7, 11-13 and 15 are rejected under 35 U.S.C. 102(e) as being anticipated by Watanabe et al (Fig. 1).

Regarding claims 1, 7, 11-13 and 15, Watanabe et al (Fig. 1) discloses an amplifier circuit comprising at least one signal amplifying transistor (40) which is coupled between an input terminal (12) and an output terminal (50), and a bypass switch (22) which is coupled to the at least one signal amplifying transistor (40) wherein the gain mode operation (amplifying stage), the two transistors (24, 26) of the bypass switch (22) are off and the at least one signal amplifying transistor (40) amplifies the received input signal (SIN) and passes the amplified signal (SOUT) to the output terminal [(50) see column 2, lines 31-37] and wherein in the bypass mode operation (not amplifying stage), the two transistors (24, 26) of the bypass switch (22) are on and the at least one signal amplifying transistor (40) is turned off and the received input signal (SIN) is passed directly from the input terminal (12) to the output terminal [(50) see column 2, lines 31-37].

Regarding claim 2, Watanabe et al (Fig. 1) further includes a controller (20) which is coupled to the at least one signal amplifying transistor (40) through the bypass switch 22.

Regarding claim 3, the controller (20) is turned off the transistors (24, 26) during the bypass mode operation (see column 2, lines 31-37).

Regarding claim 4, Watanabe et al (Fig. 1) further includes an inductor (42) which is coupled between an emitter terminal (emitter of 40) of at least one signal amplifying transistor (40) and ground (ground).

Regarding claim 5, Watanabe et al (Fig. 1) further includes an output impedance matching network (44) which is coupled to the at least one signal amplifying transistor (40) and the output terminal (50).

Regarding claim 6, Watanabe et al (Fig. 1) further includes an input impedance matching network (14) which is coupled to the at least one signal amplifying transistor (40) and the input terminal (12).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 9, 10 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Watanabe et al (Fig. 1).

Regarding claims 9 and 10, Watanabe et al (Fig. 1) discloses all the limitations in the claims except for that the amplifier is implemented in BiCMOS technology or CMOS technology. It would have been obvious to one of ordinary skill in the art at the time the invention was made to have substituted well known art-recognized equivalent transistors such as the BiCMOS or CMOS in place of the FET in the circuit of the Watanabe et al (Fig. 1) because such a modification would have been considered a mere substitution of art-recognized equivalent transistors.

Regarding claim 14, Watanabe et al (Fig. 1) discloses all the limitations in the claim 14 except for that the portion of the receiver is implemented as an integrated circuit. It is well known to those of ordinary skill in the art to integrate a semiconductor device in order to form a small sized integrated Circuit. Therefore, it would have been obvious to have integrated the circuit of the Watanabe et al (Fig. 1) because such a modification would have advantageously produced a small size integrated circuit amplifier.

Allowable Subject Matter

Claim 8 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Patent numbers (6,680,647; 6,351,183; 6,175,274; 5,399,927) are the amplifiers with the bypass switches.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Henry Choe whose telephone number is (571) 272-1760.

HENRY CHOE
PRIMARY EXAMINER

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